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EXAMINER	
MOORE, IAN N	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/873,793	ENAM ET AL.	
	Examiner	Art Unit	
	Ian N Moore	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 7-12* is/are rejected.

7)☒ Claim(s) *3-6 and 13-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/02,7/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because the do not clearly show "a method of detecting bit stream" (claim 1 and 12) and "a data transition identifier circuit" (claim 7). Although, there are several drawings that seemed to support the applicant claimed features, it is suggested to revise the drawing(s) so that clearly point out the specific drawing(s) where the claimed features are showed.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract contains the phrase, "**The invention**...", which can be implied.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: **Data transition Identifier for a network bit stream**.

Claim Objections

4. Claims 1-7 and 12 are objected to because of the following informalities:

a. **Claim 1** recites, "generating a first output in response to **detecting a first pattern**" in line 18 and "generating a forth output in response to detecting **a first pattern**" in line 12. For clarity, it is suggested to define the differences between a first output and a fourth output since both are generated identically in response to detecting a first pattern.

b. **Claim 2** recites the limitation " **the** fourth pattern" in line 20. For clarity, it is suggested to revise the limitation since there is no basis for the limitation.

c. **Claim 3** recites, "multipliercorresponding" in line 2. It is suggested to add a space between "multiplier" and "corresponding" (i.e. "multiplier corresponding").

d. **Claims 4-6** are also objected for the same reason as stated above in claim 3.

e. **Claim 7** recites the limitation "**the** fourth collector" in line 28. For clarity, it is suggested to revise the limitation since there is no basis for the limitation.

f. **Claim 12** recites, "the second input" in line 27. For consistency, it is suggested to add "data" between "second" and "input" (i.e. the second data input).

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishikawa (U.S. 6,477,184) in view of Durec (U.S. 6,100,721).

Regarding Claim 1, Ishikawa discloses a method of detecting bit transitions in a serial data stream (see FIG. 1, Demultiplexer 7 in the receiver 10), the method comprising:

demultiplexing a first bit from the serial data stream (see FIG.4 and 5, D-F/F 72-1 demux the first bit from the first channel of the incoming data stream; see col. 4, lines 50 to col. 5, lines 1-24);

demultiplexing a second bit from the serial data stream (see FIG. 4 and 5, D-F/F 72-2 demux the second bit from the second channel of the incoming data stream; see col. 5, lines 1-24), the second bit adjacent to the first bit (see FIG. 4 and 5; first bit and second bit are adjacent to each other; see col. 4, lines 54-67; col. 5, lines 30-40);

receiving a recovered clock signal (see FIG. 4 and 5, ¼ CLOCK 700), the recovered clock signal generated at least in part based on the serial data stream (see col. 5, lines 10-30; 60-65; a clock signal is generated in order to synchronize on the received data stream);

in response to the recovered clock signal, initiating pattern detection of a pattern defined by the first bit and the second bit (see FIG. 6-7, detecting and demultiplexing the first and second bit according to the clock signal; see col. 5, lines 30 to col. 6, lines 20).

Ishikawa does not explicitly disclose generating a first output in response to detecting a first pattern defined by the first bit and the second bit; generating a first output in response to detecting a first pattern defined by the first bit and the second bit; generating a second output in response to detecting a second pattern defined by the first bit and the second bit; generating a third output in response to detecting a third pattern defined by the first bit and the second bit; and generating a fourth output in response to a detecting first pattern defined by the first bit and the second bit.

However, Durec teaches in response to the recovered clock signal (see FIG. 3, Reference Frequency), initiating pattern detection of a pattern defined by the first bit and the second bit (see FIG. 3, counter 54; see col. 4, lines 25-35; the counter detects the pattern and counts the first bit and second bit);

generating a first output (see FIG. 3, output U1 or D1) in response to detecting a first pattern (see col. 3, lines 65 to col. 4, lines 6; bit pattern 00) defined by the first bit and the second bit (see col. 3, lines 65 to col. 4, lines 6, 35-30; bit pattern "00" where the first bit is "0" and the second bit is "0");

generating a second output (see FIG. 3, output U2 or D2) in response to detecting a second pattern (see col. 3, lines 65 to col. 4, lines 6; bit pattern 11) defined by the first bit and the second bit (see col. 3, lines 65 to col. 4, lines 6, 35-30; bit pattern "11" where the first bit is "1" and the second bit is "1");

generating a third output (see FIG. 3, output U3 or D3) in response to detecting a third pattern (see col. 3, lines 65 to col. 4, lines 6; bit pattern 10) defined by the first bit and the second bit (see col. 3, lines 65 to col. 4, lines 6, 35-30; bit pattern "10" where the first bit is "1" and the second bit is "0"); and

generating a fourth output (see FIG. 3, output U4 or D4) in response to a detecting first pattern (see col. 3, lines 65 to col. 4, lines 6; bit pattern 00) defined by the first bit and the second bit (see FIG. 3, counter 54; see col. 4, lines 25-35; bit pattern "00" where the counter detects the pattern and counts the first bit and second bit). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the generating different output in accordance with the specific bit pattern, as taught by Ishikawa in the system of Durec, so that it would provide the extended operating range of a phase detector beyond a phase different; see Durec col. 1, line 5-39.

Regarding Claim 2, Durec discloses wherein the acts of detecting the first pattern, the second pattern, the third pattern, and the fourth pattern are performed with substantially matched delays (see col. 3, lines 43 to col. 4, lines 55).

Regarding Claim 12, Ishikawa discloses a data transition detection circuit used to detect transitions in a serial bitstream (see FIG. 1, Demultiplexer 7 in the receiver 10), the data transition detection circuit comprising:

a first data input configured to receive a first serial bitstream data bit (see FIG. 4 and 5, D-F/F 72-1 demux the first bit from the first channel of the incoming data stream; see col. 4, lines 50 to col. 5, lines 1-24);

a second data input configured to receive a second serial bitstream bit (see FIG. 4 and 5, D-F/F 72-2 demux the second bit from the second channel of the incoming data stream; see col. 5, lines 1-24), the second serial bitstream bit adjacent to the first serial bitstream data bit, wherein the second input has substantially the same loading as the first data input (see FIG. 4 and 5; first bit and second bit are adjacent to each other; see col. 4, lines 54-67; col. 5, lines 30-40);

a timing input (see FIG. 4 and 5, ¼ CLOCK 700), configured to receive a timing signal used to initiate the detection of a data transition (see col. 5, lines 10-30; 60-65; a clock signal is generated in order to initiate the synchronizing of data transition).

Ishikawa does not explicitly disclose a first output configured to provide an indication that the first serial bitstream data bit has a value of zero and that the second serial bitstream data bit has a value of zero, wherein a first delay from the first data input to the first output is substantially the same as a second delay from the second data input to the first output; a second output configured to provide an indication that the first serial bitstream data bit has a value of one and that the second serial bitstream data bit has a value of one, wherein a second delay from the first data input to the second output is substantially the same as a third delay from the second data input to the second output; a third output configured to provide an indication that the first serial bitstream data bit has a value of one and that the second serial bitstream data bit has a value of zero; a fourth output configured to provide an indication that

the first serial bitstream data bit has a value of zero and that the second serial bitstream data bit has a value of one.

However, Durec teaches a first output (see FIG. 3, output U1 or D1) configured to provide an indication (see col. 3, lines 65 to col. 4, lines 6; bit pattern 00) that the first serial bitstream data bit has a value of zero and that the second serial bitstream data bit has a value of zero, wherein a first delay from the first data input to the first output is substantially the same as a second delay from the second data input to the first output (see col. 3, lines 65 to col. 4, lines 6, 35-30; bit pattern "00" where the first bit is "0" and the second bit is "0");

a second output (see FIG. 3, output U2 or D2) configured to provide an indication (see col. 3, lines 65 to col. 4, lines 6; bit pattern 11) that the first serial bitstream data bit has a value of one and that the second serial bitstream data bit has a value of one, wherein a second delay from the first data input to the second output is substantially the same as a third delay from the second data input to the second output (see col. 3, lines 65 to col. 4, lines 6, 35-30; bit pattern "11" where the first bit is "1" and the second bit is "1");

a third output (see FIG. 3, output U3 or D3) configured to provide an indication (see col. 3, lines 65 to col. 4, lines 6; bit pattern 10) that the first serial bitstream data bit has a value of one and that the second serial bitstream data bit has a value of zero; (see col. 3, lines 65 to col. 4, lines 6, 35-30; bit pattern "10" where the first bit is "1" and the second bit is "0"); and

a fourth output (see FIG. 3, output U4 or D4) configured to provide an indication (see col. 3, lines 65 to col. 4, lines 6; bit pattern 01) that the first serial bitstream data bit has a value of zero and that the second serial bitstream data bit has a value of one (see FIG. 3,

counter 54; see col. 4, lines 25-35; bit pattern "01" where the counter detects the pattern and counts the first bit and second bit). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the generating different output in accordance with the specific bit pattern, as taught by Ishikawa in the system of Durec, so that it would provide the extended operating range of a phase detector beyond a phase different; see Durec col. 1, line 5-39.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over McGinn (U.S. 5,103,123) in view of Durec.

Regarding Claim 7, McGinn discloses a data transition identifier circuit used to identify data transitions in a network bitstream (see FIG. 1, phase detector 10), the data transition identifier circuit comprising:

a first differential input coupled to a first clock signal (see FIG. 1, Input sync signal 22; see col. 2, lines 45-50);

a second differential input coupled to a second clock signal (see FIG. 1, Input oscillator signal 24; see col. 2, lines 45-50);

true data input and inverse data input (see FIG. 1, inputs to base of the transistors);

pattern indicator output (see FIG. 1, inputs to collectors of the transistors);

a first constant current sink (see FIG. 1, current I 12; see col. 2, lines 50-56)

a second constant current sink (see FIG. 1, current I 16; see col. 2, lines 50-56);

a first transistor having a first base, a first emitter and a first collector (see FIG. 1, transistor 34 with base, emitter and collector), the first base coupled to the first differential input and the first emitter coupled to the first constant current sink (see col. 2, lines 58-65);

a second transistor having a second base, a second emitter and a second collector see FIG. 1, transistor 28 with base, emitter and collector), the second base coupled to the first differential input and the second emitter coupled to the second constant current sink (see col. 2, lines 28 to col. 3, lines 45);

a third transistor having a third base, a third emitter and a third collector (see FIG. 1, transistor 72 with base, emitter and collector), the third base coupled to the second differential input and the third emitter coupled to the first constant current sink (see col. 3, lines 10-17);

a fifth transistor having a fifth base, a fifth emitter and a fifth collector (see FIG. 1, transistor 30 with base, emitter and collector), the fifth base coupled to the first true data input, the fifth collector coupled to the pattern indicator output and the third collector, and the fifth emitter coupled to the first collector (see col. 2, lines 58 to col. 3, lines 45);

a sixth transistor having a sixth base, a sixth emitter and a sixth collector (see FIG. 1, transistor 74 with base, emitter and collector), the sixth base coupled to the inverse data input, the sixth collector coupled to the fourth collector and the pattern indicator output, and the sixth emitter coupled to the fifth emitter and the first collector (see col. 3, lines 1-17);

a seventh transistor having a seventh base, a seventh emitter and a seventh collector (see FIG. 1, transistor 92 with base, emitter and collector), the seventh base coupled to the

true data input, the seventh collector coupled to the sixth collector, and the seventh emitter coupled to the second collector (see col. 3, lines 1-45); and

a eighth transistor having an eighth base, an eighth emitter and an eighth collector (see FIG. 1, transistor 30 with base, emitter and collector), the eighth base coupled to the inverse data input, the eighth collector coupled to the fifth collector, and the eighth emitter coupled to the second collector (see col. 3, lines 1-45).

McGinn does not explicitly disclose a second true data input, a second inverse data input, a second pattern indicator output. However, Durec teaches a first true data input (see FIG. 3, Input C to 52);

a first inverse data input (see FIG. 3, inverse input D to 52);

a second true data input (see FIG. 3, Input C to 58);

a second inverse data input (see FIG. 3, inverse input C to 58);

a first pattern indicator output (see FIG. 3, output U1 or D1 at counter 54);

a second pattern indicator output (see FIG. 3, output U2 or D2 at counter 54).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a second true data input, a second inverse data input, a second pattern indicator output, as taught by Durec in the system of McGinn, so that it would provide the extended operating range of a phase detector beyond a phase different; see Durec col. 1, line 5-39.

Allowable Subject Matter

8. Claims 3-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and rewritten to overcome the objections set forth in paragraph 4.

9. Claims 8-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim.

10. Claims 13-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N Moore whose telephone number is 571-272-3085. The examiner can normally be reached on M-F: 9:00 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

INM

3/11/05

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